IN THE SPECIFICATION

Please amend the specification as follows:

After the STATEMENT OF RELATED APPLICATIONS section please add the following new paragraph **[0001]** and replace paragraphs previously numbered **[0001] – [0004]** with the rewritten paragraphs now numbered **[0002] – [0005]**:

[0001] This application is a divisional application of co-pending U.S. Patent Application 10/103,674, filed March 21, 2002, entitled "Power Semiconductor Device Having A Voltage Sustaining Region That Includes Doped Columns Formed With A Single Ion Implantation Step."

~~[0001]~~ **[0002]** This application is related to ~~copending~~ U.S. Patent Application Serial No. 09/970,972 entitled "Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer," filed in the United States Patent and Trademark Office on October 4, 2001, now U.S. Patent 6,465,304.

~~[0002]~~ **[0003]** This application is related to ~~copending~~ U.S. Patent Application Serial No. 10/039,068 entitled "Method For Fabricating A High Voltage Power MOSFET Having A Voltage Sustaining Region That Includes Doped Columns Formed By Rapid Diffusion," filed in the United States Patent and Trademark Office on December 31, 2001, now U.S. Patent 6,566,201.

~~[0003]~~ **[0004]** This application is related to ~~copending~~ U.S. Patent Application Serial No. 10/038,845 entitled "Method For Fabricating A High Voltage Power MOSFET Having A Voltage Sustaining Region That Includes Doped Columns Formed By Trench Etching and Ion Implantation," filed in the United States Patent and Trademark Office on December 31, 2001, now U.S. Patent 6,656,797.

~~[0004]~~ **[0005]** This application is related to ~~copending~~ U.S. Patent Application Serial No. 09/970,758 entitled "Method For Fabricating A Power Semiconductor Device Having A Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands," filed in the United States Patent and Trademark Office on October 4, 2001, now U.S. Patent 6,649,477.

Please replace paragraph **[0011]** with the following rewritten paragraph:

[0011] The structure shown in FIG. 3 can be fabricated with a process sequence that includes multiple epitaxial deposition steps, each followed by the introduction of the appropriate dopant. Unfortunately, epitaxial deposition steps are expensive to perform and thus this structure is expensive to manufacture. Another technique for fabricating these devices is shown in ~~copending~~ U.S. Appl. Serial No. ~~[GS 158]~~ 09/970,972, now U.S. Patent 6,465,304, in which a trench is successively etched to different depths. A dopant material is implanted and diffused through the bottom of the trench after each etching step to form a series of doped regions (so-called "floating islands") that collectively function like the p-type doped regions 40 and 42 seen in FIG. 3. However, the on-resistance of a device that uses the floating island technique is not as low as an identical device that uses continuous columns.